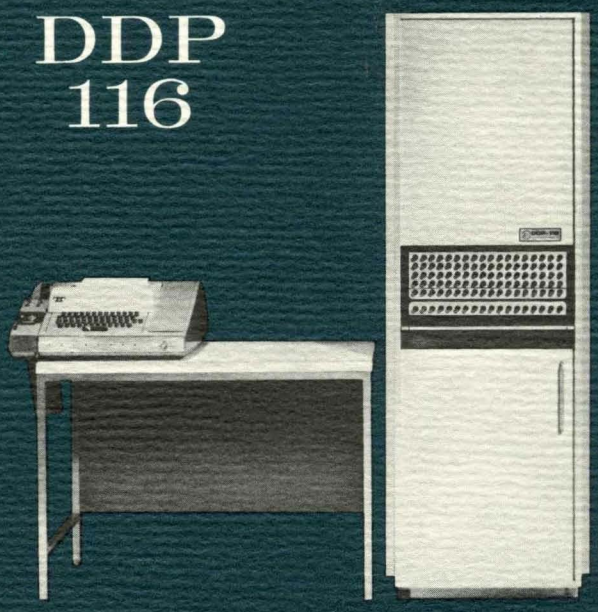
DDP 116



INTERFACE MANUAL

COMPUTER CONTROL COMPANY, INC.

Document No. 71-293

INTERFACE MANUAL
FOR
DDP-116 GENERAL-PURPOSE COMPUTER

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FOR

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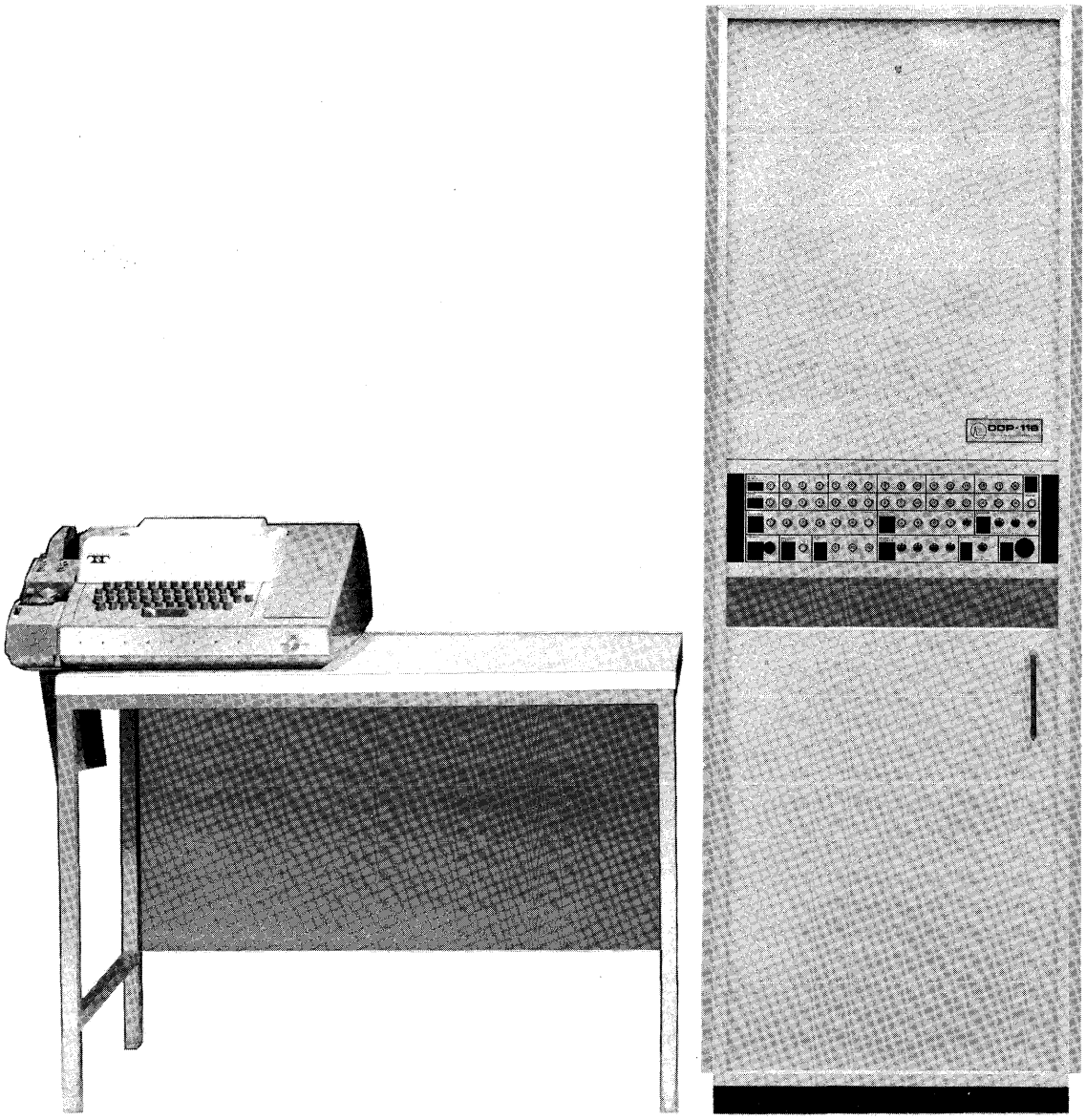

Figure 1. Standard DDP-116

DDP-116
INTERFACE MANUAL

INTRODUCTION

The DDP-116 General-Purpose Computer (Figure 1) features versatile input/output capabilities, easy expandability through modular design, a variety of input/output modes, and simplicity of operation. This manual describes and illustrates the interface characteristics of the DDP-116 to facilitate proper connection with peripheral equipment. The basic methods of input/output data transfer (Standard I/O Bus and Direct Multiplexed Channel) are described in sufficient detail for system planning purposes. Data and control lines required for input/output communications are defined, timing requirements are established, and interface gating drive and load requirements are specified. A detailed description of input/output operation is given in the DDP-116 Programmer's Manual.

DDP-116 I/O COMMUNICATION

Communication links between the standard DDP-116 and its peripheral equipment are illustrated in Figure 2. The standard machine, without options, communicates with peripheral equipment on a parallel I/O bus under program control. A separate instruction is required for every input or output word transfer. All peripheral devices (up to 18 may be attached) are tied to a single interrupt signal line. When a device requests service through the interrupt line, a programmed subroutine determines which device requires service. An optional priority interrupt system is available to eliminate the need for programmed priority determination.

The Direct Multiplexed Channel (DMC) option is a time-shared automatic I/O system that uses the parallel I/O bus for communication but performs single character or block data transfers without program intervention. DMC transfers are interleaved with computation; the starting and terminating addresses of the locations to which the block of information is to be transferred are set up initially in standard memory locations under program control. Data transfers thereafter occur at a rate of one word every 6.8 microseconds. The transfer rate is over 145,000 words per second. At slower I/O rates, any time not needed by the DMC is used for computation.

Each peripheral device used with the DDP-116 requires a suitable control interface compatible with the standard parallel I/O bus. The control interface must be capable of decoding device addresses and function codes, must provide start-stop and control signals to the device proper, and in most cases must include a buffer register to synchronize data transfers with the DDP-116 processing cycle. Control interfaces are provided with all standard DDP-116 peripheral equipment options. In addition, general-purpose control interfaces are available as standard options for use with special devices, or special control in-

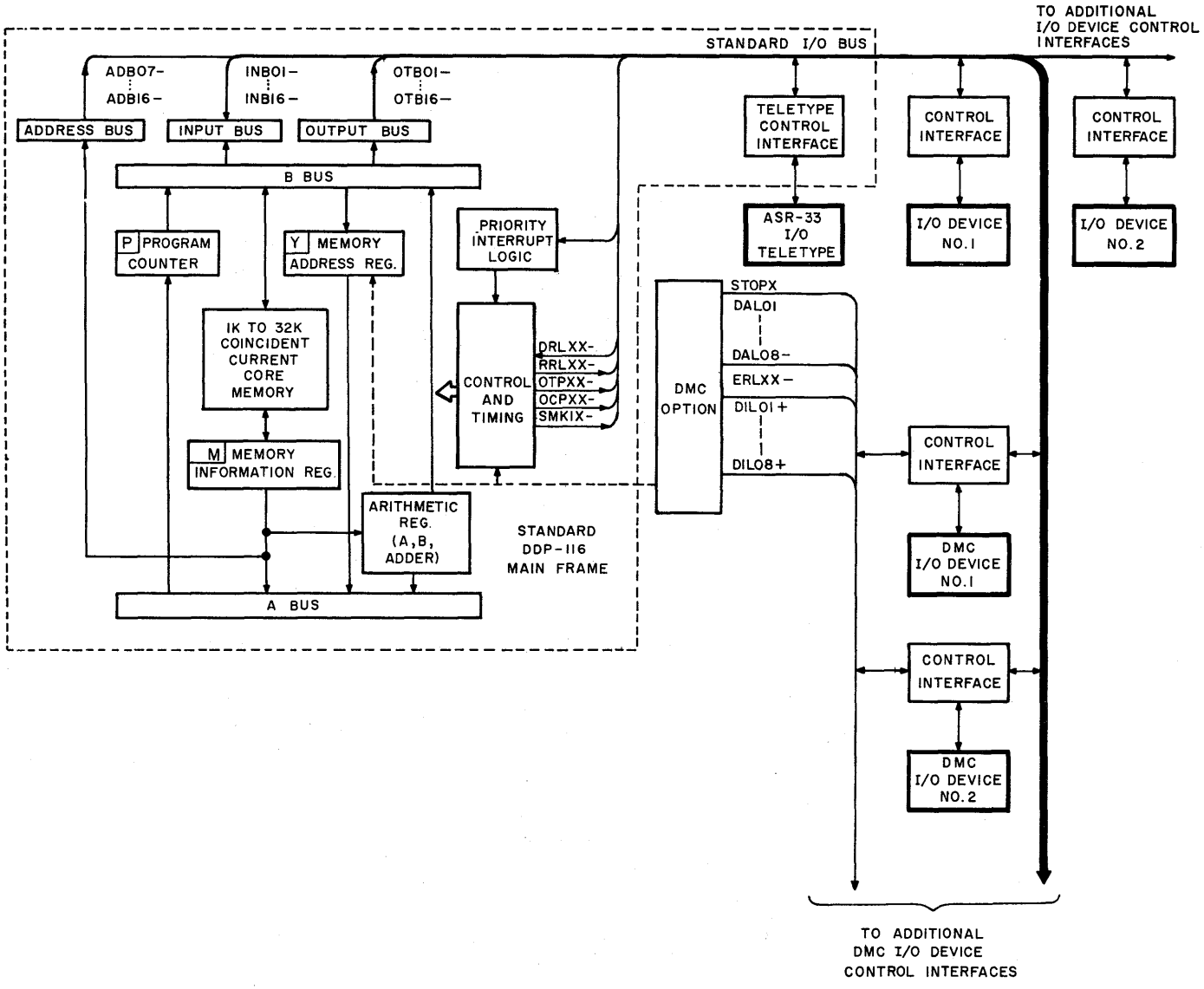

Figure 2. DDP-116 I/O, Block Diagram

terfaces can be designed. The following information will enable a user to design any device or communication link control interface compatible with the DDP-116 bus structure, from the standpoints of timing, logic levels, and circuit loading.

STANDARD PARALLEL I/O BUS

Standard I/O Bus Lines

The standard DDP-116 input/output mode consists of transfers of single characters or 16-bit words to and from the data processor B bus. Input transfers are performed by INA instructions, and output transfers by OTA instructions. Communication with peripheral devices is accomplished by using an Input/Output Bus, consisting of the following elements: 10 address lines (ADB07 through ADB16); 16 input data lines (INB01 through INB16); 16 output data lines (OTB01 through OTB16); and a series of control lines (OCP, SMK, RRL, OTP, DRL, and PIL). The data processor distinguishes between devices (with respect to the destination of commands or the source or destination of data transfers) by a six-bit binary code on the address bus. Up to 18 devices may be paralleled on the common bus.

Logic Levels

Standard logic levels for S-PAC circuits are 0 volt for logical ZERO and -6 volts for logical ONE. Negative logic is used in DDP-116 I/O communication to permit ORing of I/O bus levels. All active signals (command pulses and binary ONE bits in data and address codes) are transmitted at the current-driving 0-volt level. Binary ZEROs and quiescent control signals rest at the -6-volt level for minimum current drain.

Timing of the address, data, and command lines from the DDP-116, and timing requirements imposed on responses from the device control units, are conditional upon the instruction in effect. Table 1 provides I/O bus line functions for the operational modes peculiar to I/O processing. Each of the modes is described in detail in the following paragraphs.

OCP Commands

OCP commands initiate motion of a device or prepare it for a specific mode of operation. No data is exchanged, and no response signal is expected from the addressed device. Only the address bus lines and the OCPXX-command pulse are involved. OCP command timing is shown in Figure 3.

The device address code and function code are gated from OCP instruction word positions 7 through 16 to the corresponding bit positions of the address bus. During the last half of the address interval, the OCPXX-command pulse occurs to enable the addressed device to perform the control function specified by the function code portion of the address. No direct response is required of the device. Any information placed by the device on DRLXX- or INB01 to INB16 will be ignored by the computer during this instruction. Execution of the OCP command is verified during the sensing portion of a subsequent SKS,

Table 1.
Single Word Transfer I/O Bus Signal Functions

Control or Data Line	Function					
	OCP	SKS	INA	OTA	Set Mask	Interrupt
OTB_{1-16}				Contains data	Contains mask status code	
INB_{1-16}			Device applies data			
ADB_{7-10}	Function code	Function code	Function code	Function code	Unique code	
ADB_{11-16}	Device address	Device address	Device address	Device address	Unique code	
OTP				Strobes data to device buffer		
DRL		Device replies if condition determined by function code is TRUE	Device replies if ready	Device replies if ready		
RRL			Resets device ready flip-flop	Resets device ready flip-flop		
OCP	Sets mode determined by function bits					
SMK1					Strobes mask bits to mask flip-flops	
PIL						Asynchronous signal originating in device interface demands priority interrupt

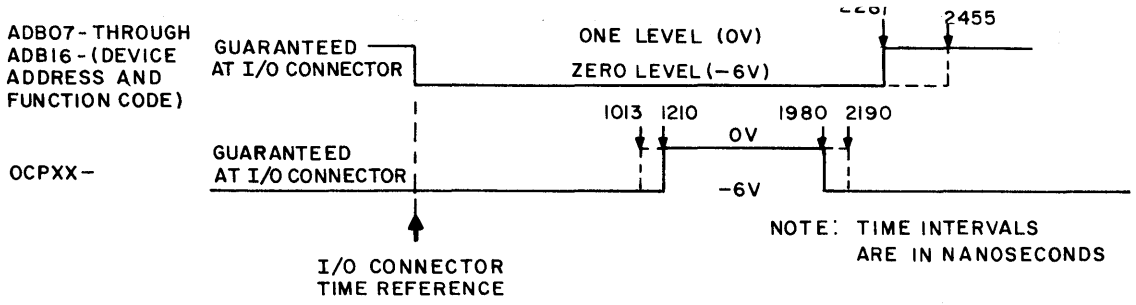

Figure 3. OCP I/O Command, Timing Diagram

INA, or OTA instruction cycle.

Typical uses of the OCP command are to:

a. turn the high-speed paper tape punch on or off,

b. set up the binary or BCD mode in the paper tape reader, and

c. rewind magnetic tape.

SKS Commands

The SKS command is used to test the condition of any device connected to the standard I/O bus. The command is implemented by gating the devices address onto the address bus with a function code that identifies the condition being tested. If the condition is true, the device interface must bring the DRLXX- line to the 0-volt level during the time limits specified in Figure 4. The DRLXX- signal causes a program skip to the next instruction in sequence. If the DRLXX- line remains quiescent, the next instruction in sequence is executed.

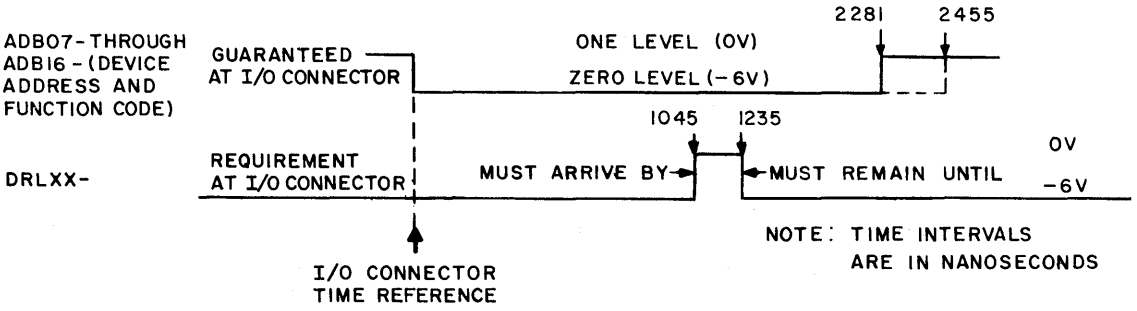

Figure 4. SKS Sensing Command, Timing Diagram

INA Commands

An INA command addresses a particular device and senses the device condition. If the device replies with a "ready" indication, the input bus is strobed to the DDP-116 A register. Timing is illustrated in Figure 5. The address and function code are placed on the address bus. Within 1.2 microseconds after receiving the address, the device must bring the DRLXX-line to the "ready" condition (0 volt level). Otherwise, the DDP-116 ignores the data on the lines and continues with the normal porgram. If the "ready" condition is detected, data on the input bus is strobed to the A register and the next instruction in sequence is skipped.

While data is being strobed into the A register, a reset ready pulse (RRLXX-) is sent out from the computer to indicate that the information has been accepted. This signal may be used to dc reset the ready flip-flop in the control interface. The device must apply data to the input bus within 2.3 microseconds after receiving the address.

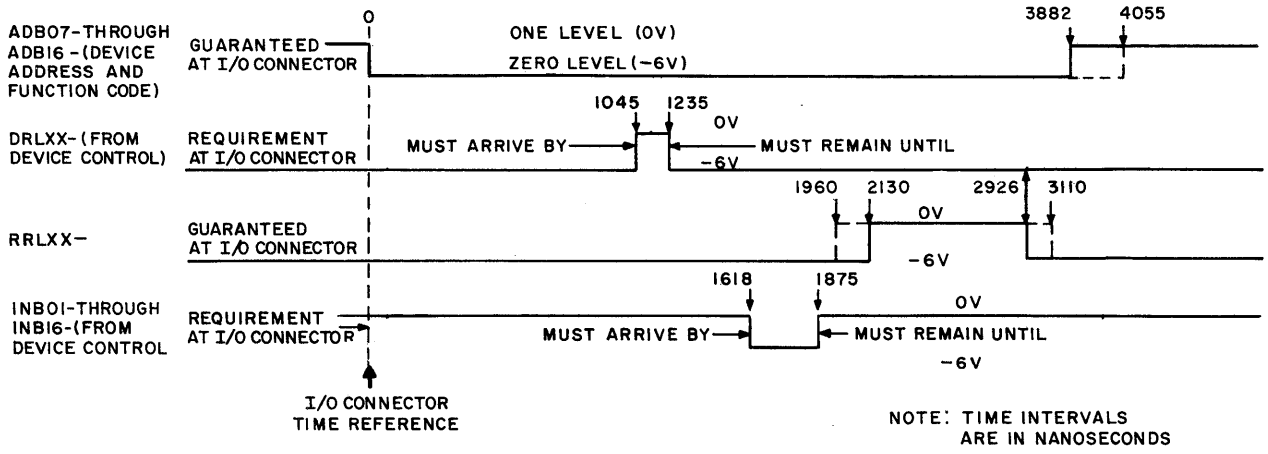

Figure 5. INA Input Data Transfer, Timing Diagram

OTA Commands

During an OTA output command, the device address and data are applied to the address and output bus lines. The device's ready status is sensed and if the device is prepared to receive the data, the OTPXX- pulse is generated to strobe the data to the device buffer. If the device is not ready, no strobing occurs, and the DDP-116 program continues on the assumption that the data transfer was not performed. Timing is illustrated in Figure 6.

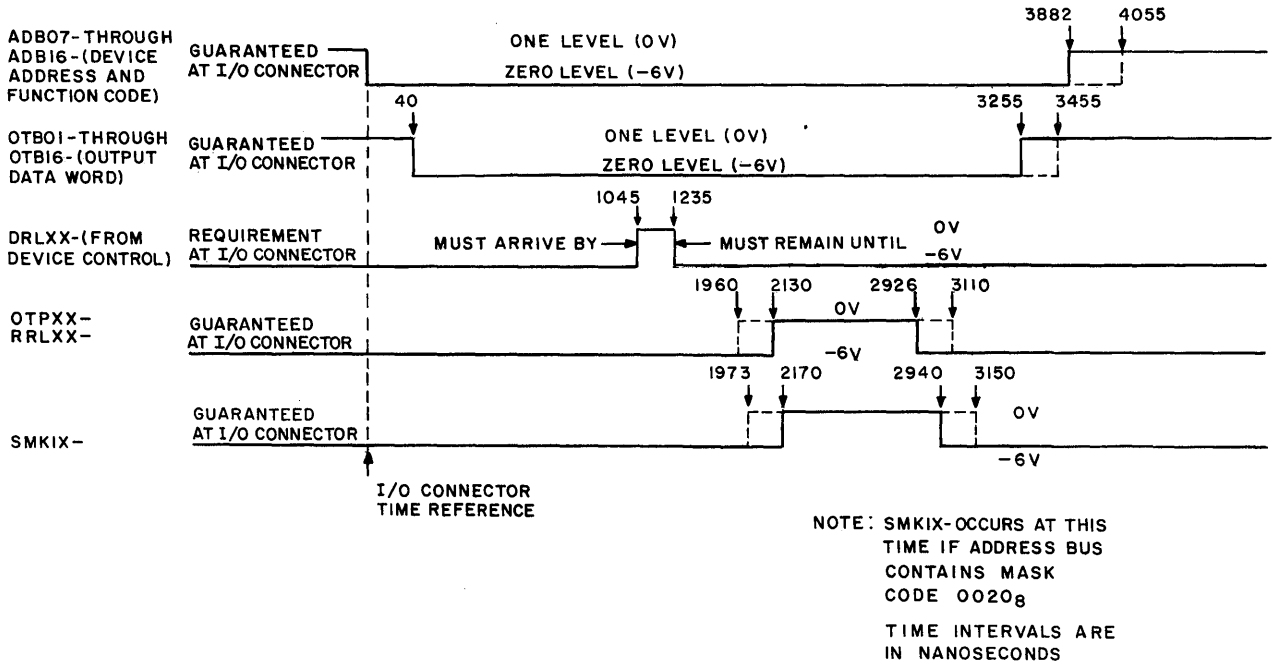

Figure 6. OTA Output Data Transfer, Timing Diagram

Within 1.12 microseconds after receiving the address, the device must respond by bringing the DRL line to the "ready" condition (0 volt level). Otherwise, the program continues on the basis that data was not accepted. If a "ready" condition is detected, the DDP-116 responds with the OTPXX- pulse, which enables the device to strobe the output data lines to the device buffer. A reset ready pulse (RRLXX-) is sent out concurrently with the OTPXX- pulse. Its trailing edge may be used to reset the ready status of the device.

Standard Interrupt Provisions

Interrupt masks are set and reset by a variant of the OTA instruction, in which the device address and function code portion of the instruction word are replaced by the arbitrary code 0020_8. All devices respond to the code by monitoring the output bus, which contains a mask-setting code derived from the A register. If a device detects a binary ONE (0 volt level) in its preassigned position, a mask flip-flop is set, and the device can call for service on the PILXX- line. If a device detects a binary ZERO in its preassigned position, a mask flip-flop is reset. The PILXX- level diverts the DDP-116 to a priority-determining subroutine that performs SKS interrogations in the order of priority until the busy channel is detected.

Timing of the mask-setting instruction is illustrated in Figure 6. The address lines and output bus are generated as in an OTA instruction. When the peculiar mask-setting code is specified in the instruction word format, the SMK1X- pulse is generated. No DRLXX- response is required.

Once the mask flip-flop is set, the device interface asynchronously requests interrupt service by raising the PILXX-line. The computer responds by issuing a series of SKS instructions encoded to detect the device causing interrupt. Each device interface must contain a decoder to sense the "SKS interrupt" command and respond on the DRLXX-line. If a device is not interrupting, it returns a 0 volt level on the DRLXX- line (see Figure 4) to cause a program skip to an "SKS interrupt" for the next lower priority. If the device is interrupting, the DRLXX-line is held at the -6 volt level during the SKS command, and the program counter can process the next sequential instruction, which will refer to a subroutine appropriate to the interrupting device.

Gating Circuit Characteristics

All data and control signals from the DDP-116 I/O bus to the device controls are driven by standard Computer Control Company type PN-30 non-inverting power amplifiers. (See Figure 7.) Each amplifier is capable of driving loads of up to a total of 96 ma maximum and up to 2000 pf in the power-driving state (0 vdc). Because several device interfaces may be connected in parallel on the I/O bus lines, it is recommended that no device present a load of more than 2.4 ma at 0 volt to a given line. This particular requirement can be disregarded in a special system application so long as the total current limit is not exceeded.

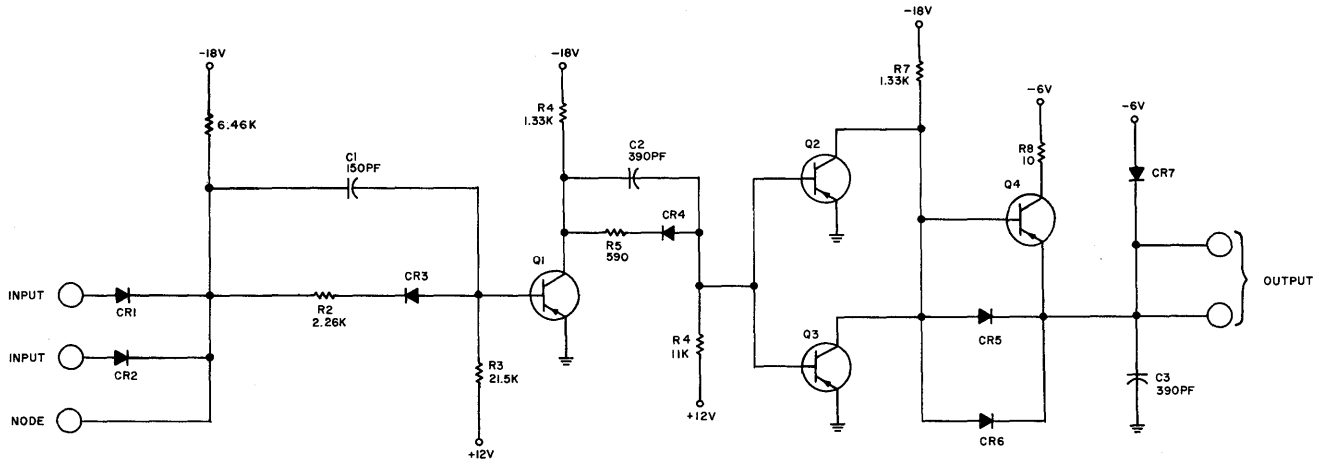

Figure 7. Non-Inverting Power Amplifier PAC, Model PN-30, Schematic Diagram

All input lines from device interfaces to the DDP-116 drive line terminations in a Special PAC. (See Figure 8.) These termination circuits operate as collector loads for the driving circuit and correspond to 3.2 ma at 0 volt. No external collector loads are to be used. Rise and fall times of input signal levels are not critical as long as the 90 percent and 10 percent levels occur within the time limitations shown in Figures 3, 4, 5, and 6.

Specifications for the I/O bus lines from the standpoint of a single device interface are summarized in Tables 2, 3, 4, and 5. For signals originating in the DDP-116, the information is descriptive; it indicates what will be delivered to the I/O connector panel. For signals originating at the device interface, the information is prescriptive; it indicates the limits to which the device interface must conform for compatibility with DDP-116 internal organization.

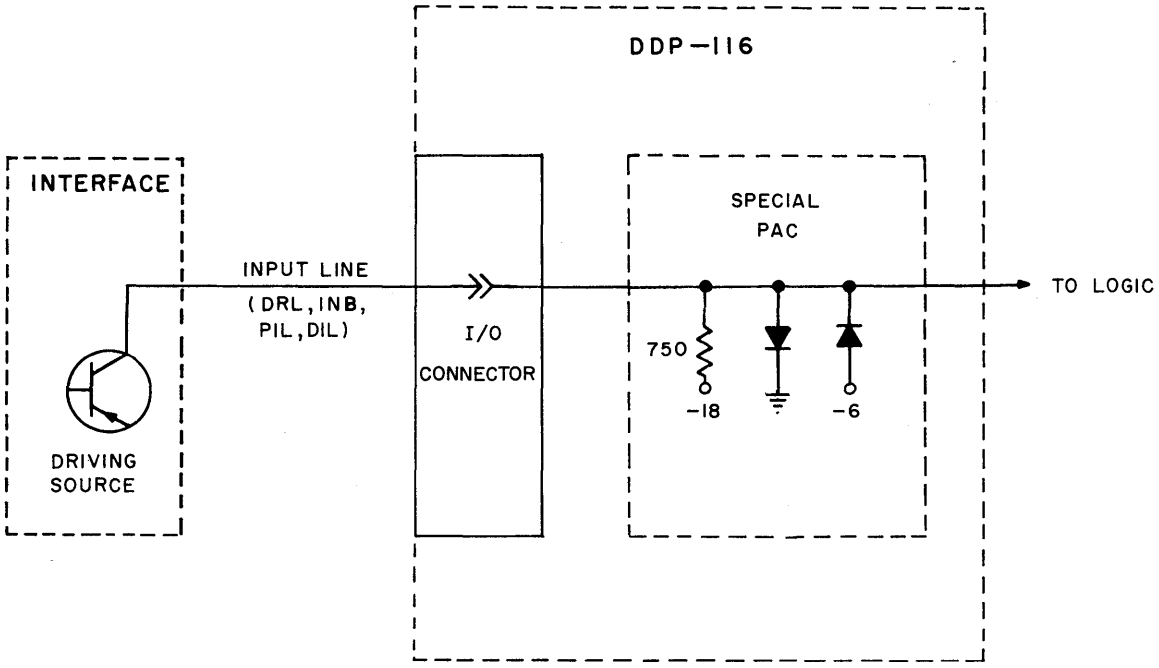

Figure 8. Input Line Termination, Schematic Diagram

Table 2.
ADB07- to ADB16- and OTB01- to OTB16- Signal Characteristics

Binary ONE:	0 volt to -1.5 volts
Binary ZERO:	-5.5 volts to -6.5 volts
Output loading:	96 ma and 2000 pf maximum per line at ONE level Loading per device not to exceed 2.4 ma per line at ONE level
Rise time:	200 ns from 10% to 90% points at DDP-116 I/O connector (nominal)
Fall time:	500 ns from 90% to 10% points at DDP-116 I/O connector (nominal)
Pulse specifications:	See Figures 3, 4, 5, and 6.

Table 3.
OTPXX-, RRLXX-, OCPXX-, and SMK1X- Signal Characteristics

Active level:	0 volt to -1.5 volts
Quiescent level:	-5.5 volts to -6.5 volts
Output loading:	96 ma and 2000 pf maximum per line at active level Loading per device not to exceed 2.4 ma per line at active level
Rise time:	200 ns from 10% to 90% points at DDP-116 I/O connector (nominal)
Fall time:	500 ns from 90% to 10% points at DDP-116 I/O connector (nominal)
Pulse specifications:	See Figures 3, 5, and 6.

Table 4.
INB01- to INB16- Signal Characteristics

Binary ONE:	0 volt to -1.5 volts
Binary ZERO:	-5.5 volts to -6.5 volts
Input loading by DDP-116:	3.2 ma at ONE level for each line Negligible current at ZERO level
Timing:	See Figure 5. Rise and fall times are unimportant provided overall timing is satisfied at DDP-116 I/O connector

Table 5.
DRLXX- and PILXX- Signal Characteristics

Active level:	0 volt to -1.5 volts
Quiescent level:	-5.5 volts to -6.5 volts
Input loading by DDP-116	3.2 ma at active level for each line Negligible loading at quiescent level
Timing:	For DRLXX-, see Figures 4, 5, and 6. Rise and fall times are unimportant if overall timing is satisfied at DDP-116 I/O connector
	PILXX- is generated asynchronously by the device interface. Rise and fall times of less than 1.5 μsec are recommended for optimum utilization of computer interrupt cycles

DIRECT MULTIPLEXED CHANNEL (DMC) OPTION

The DMC hardware option permits medium-speed and high-speed I/O transfers with a minimum of programmed control. Data transfers are performed by using the standard I/O bus and its control lines, but interrupts are initiated and I/O transfers are controlled by the DMC logic rather than by programmed INA or OTA instructions. When a device controlled by the DMC requests service, the DMC stops the program at the end of the current instruction and holds the computer in the D-state. During the D-state, a passive state during which normal computer cycles are suspended, the DMC performs a four-cycle simulated instruction that accomplishes the I/O transfer.

During the four 1.7 μsec cycles of the DMC sequence (G-cycle, H-cycle, J-cycle, and K-sync cycle), the DMC option assumes control of the computer memory and uses DDP-116 registers and the arithmetic capability to access or store data. The current program count and accumulator contents are preserved; at the end of the DMC sequence, the computer is returned to the F-cycle of the next instruction unless a new interrupt has occurred. Preassigned memory locations for each of the eight DMC channels must be set up with starting address minus one and end address, through normal programmed instructions. Devices must also be set up for the desired modes of operation by OCP commands, as in standard I/O transfers. Also, a device must be set up for DMC mode by a special OCP, $03XX_8$. Once these preliminary setups are made, I/O transfers occur on demand from the device, without program intervention.

The DMC has two basic modes of operation, time-sharing mode and block transfer mode, established by control bits stored with the starting address for each channel. The essential difference between the two modes is that, in the time-sharing mode, control reverts to the computer after an unsuccessful sync cycle, whereas in the block transfer mode the DMC retains control and repeats its sync cycle until a new demand occurs. The block transfer mode is essential in the case of a high-speed device operating only slightly slower than the maximum transfer rate. During the occasional failure to synchronize, the device

is still in motion; if the computer assumed control for several cycles, data would be lost. Devices operating in the block transfer mode should be given the highest priorities; otherwise, other channels not in the block transfer mode might interrupt and cause data loss. When the block transfer mode has been set up for a particular channel, it is sustained until the channel reaches the end of range or is disabled by a stop command originating in the device control interface. If a device runs out of data before the end of range is reached, the stop command resets the block transfer mode in the DMC and permits the computer to resume control.

During normal computer operation, the DMC repeats its 1.7 μsec sync-cycle in synchronization with every computer cycle. If any of the eight channels becomes active during a sync-cycle, a priority evaluation is made and the highest priority is selected. The DMC is then ready to interrupt the computer, but the computer in turn permits DMC interrupt only during the last cycle of an instruction. If the computer does not accept the interrupt (for example, during the second cycle of a three-cycle instruction, such as OTA), the DMC is reset and a new priority determination occurs during the next sync-cycle. Thus it is possible for a device that was waiting for access during the unsuccessful sync-cycle to be superseded by a newer request from a device of higher priority.

When the interrupt demand is accepted, an address peculiar to the selected DMC channel is forced into the memory address register so that the memory cycle initiated as the last step of the instruction fetches the channel starting address rather than the next instruction word. The computer is arrested in the D-state, and the DMC, taking control, enters its G-cycle. During the G-cycle, the device is addressed and the starting location address is updated. An H-cycle follows, in which the end address is fetched. Next, a J-cycle occurs, to perform the actual data transfer (using the standard I/O bus and appropriate control lines). The final K-sync cycle repeats the function of the sync cycle and also compares the updated starting address with the end address. If they are identical, an end-of-range pulse is sent to the device to stop its operation. The K-sync cycle ends with a return of control to the computer, starting with the fetch cycle that was interrupted by the D-state. The DMC returns to its passive sync cycle until a new interrupt is sensed.

The basic control interfaces for DMC-controlled devices are logically identical to those used with the standard I/O bus, but additional logic must be added to accommodate the DAL address lines, DIL interrupt lines, ERL end-of-range line, and STOPX- device stop line. The timing and the characteristics of these additional signals are described in the following paragraphs.

I/O Transfers

Timing of the DMC sequence for input/output devices is shown in Figure 9. When an active DIL request is detected during a DMC sync cycle that concurs with the last cycle of an instruction (one that would be followed by an F-cycle), DMC interrupt is enabled. If more than one device is requesting service, a DMC priority scheme selects the device with the

highest priority by enabling an address signal on the appropriate DAL line. The DAL signal appears on the address lines early in the DMC G-cycle; its leading edge establishes a zero time reference for all subsequent events.

Upon receiving the address, the requesting device interface inhibits its DIL line. Otherwise, the DIL line would remain high through the K-sync cycle and would erroneously enable a second DMC transfer to the same device.

For input transfers, data from the device must be placed on the input bus by T1 of the DMC J-cycle and must remain through T3. It is conventional to reset input data by the end of the RRLXX-pulse, though data could be sustained through the end of the DMC sequence without conflict. The resetting of the device ready flip-flop by the RRLXX-pulse indicates that data has been accepted and that it is permissible to clear the buffer. The device DIL line is disabled as another consequence. The OTPXX-pulse is not generated by the DDP-116 during an input cycle, and the output bus remains inactive.

For output transfers, the device buffer must be clear by T3 of the DMC J-cycle. Data is applied to the output bus during the time interval illustrated in Figure 9 and is strobed to the buffer by the OTPXX-pulse. The ready flip-flop is reset, and the PIL line is disabled by the RRLXX-pulse.

By the beginning of the DMC K-sync cycle, the input or output data transfer is complete, and the device interface is prepared for a new character. During the K-sync cycle, the updated data address is compared with the end address of the assigned block. If the end address has been reached, the DMC is inhibited from addressing data transfers to the device. A new priority determination is made, as during a sync cycle. The same device cannot cause a consecutive D-state, because its DIL line has been held off through the beginning of the K-sync cycle. If the DIL line of another device has been energized in time, however, the DMC retains control, the computer D-state is sustained, and another DMC transfer sequence occurs. If no new device is interrupting and the DMC is in time-sharing mode, control reverts to the computer for at least one full instruction cycle. In the block transfer mode, the D-state is sustained, DMC control remains in effect, and sync-cycles are repeated until an interrupt is detected.

When the end of range is detected during the K-sync cycle, the DAL line to the addressed device is sustained for an extra microsecond to gate the ERLXX- end-of-range pulse to the device controls, to turn off the "DMC ready" flip-flop. Because of the sustained address, no new interrupt is permitted even if a DIL line has been energized in time. Control is returned to the computer for at least one instruction cycle.

Special DMC Signal Gating Circuit Characteristics

Signals from the DMC option to the associated device interfaces are gated by standard Computer Control Company type PN-30 non-inverting power amplifiers (Figure 7), as are the standard I/O bus output lines. The DIL input from each interface drives a type S-330 transfer gate. (See Figure 10.) Specifications for the additional DMC control lines from the standpoint of a single device interface are listed in Tables 6 and 7.

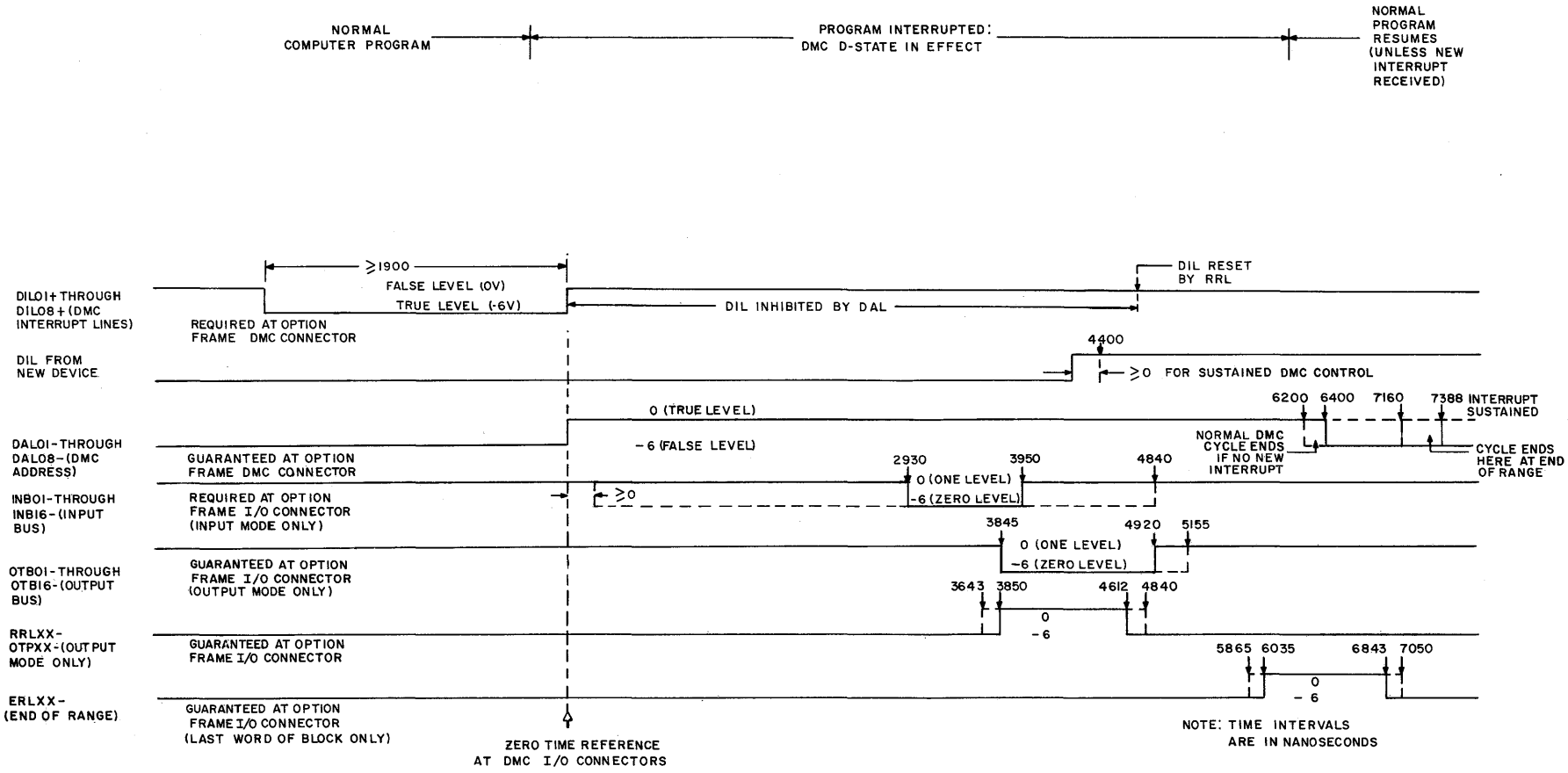

Figure 9. DMC I/O Transfer, Timing Diagram

Table 6.
ERLXX- and DAL01- through DAL08- Signal Characteristics

Active level:	0 volt to -1.5 volts
Quiescent level:	-5.5 volts to -6.5 volts
Output loading:	96 ma and 2000 pf maximum per line at active level Loading per device not to exceed 2.4 ma per line at active level
Rise time:	200 ns from 10% to 90% points at option rack I/O connector (nominal)
Fall time:	500 ns from 90% to 10% points at option rack I/O connector (nominal)
Pulse specifications:	See Figure 9.

Table 7.
DIL01+ through DIL08+ Signal Characteristics

Active level:	-5.5 volts to -6.5 volts
Quiescent level:	0 volt to -1.5 volts
Input loading by DMC:	3.2 ma at active level for each line Negligible loading at quiescent level
Timing:	See Figure 9. DIL lines are generated asynchronously by the device interfaces. Rise and fall times of less than 1.5 μsec are recommended for optimum utilization of DMC interrupt cycles.

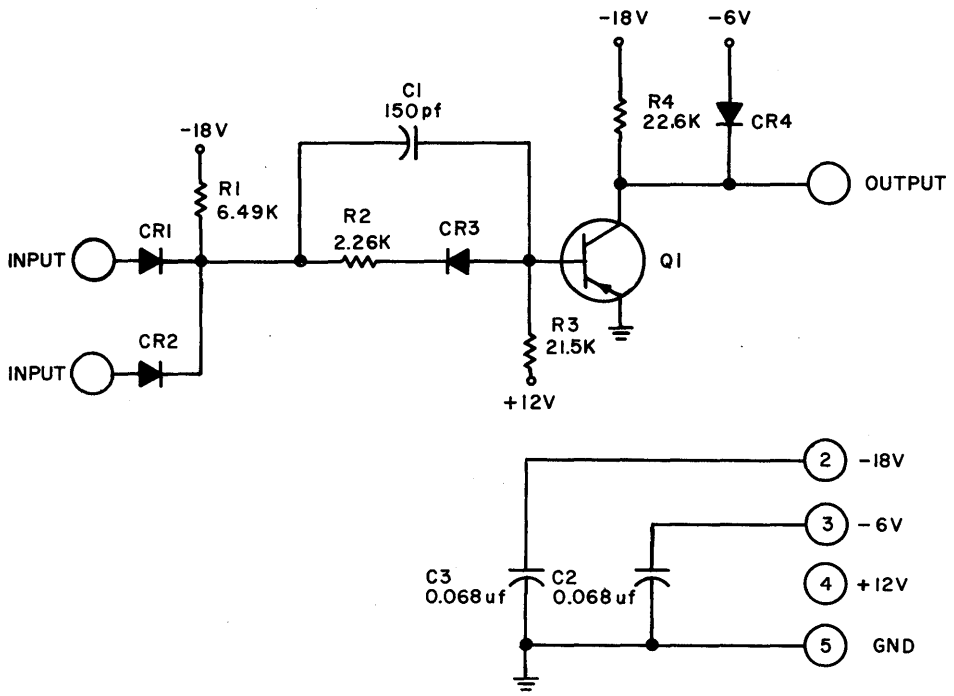

Figure 10. Transfer Gate PAC, Model S-330, Schematic Diagram

PRIORITY INTERRUPT OPTION

The priority interrupt hardware option eliminates the need for a programmed subroutine to identify the device requesting service. Identification is necessary because all device interface PIL lines are ORed to a common bus. In the priority interrupt option, PIL lines from up to eight different devices are applied to independent loads. When more than one interrupt demand occurs, the one having the highest priority is selected by prewired logic, and a unique jump destination address is made available to the DDP-116. Synchronization is achieved during the next available computer fetch cycle, when the jump destination is gated to the memory address register and a JST operation code is forced into the F register. The computer proceeds as if an indirect JST instruction had been fetched. The destination, in this case, is the first program step of a subroutine suitable for I/O transfer to or from the interrupting device. The program count current at the time of the interrupt is retained, and when the I/O transfer is complete, the normal program is resumed. Subroutines for interrupt I/O transfers may themselves be interrupted by a demand from a device of higher priority.

In order to initiate an interrupt demand, a device interface must first be enabled by the setting of its mask flip-flop, as described in connection with the standard I/O bus.

Priority interrupt option units may be used in multiple in a fan-in arrangement that accommodates up to 256 PIL lines and provides as many jump destination address codes.

Loading imposed on PIL lines by the priority interrupt option input gates is identical to that imposed by the DDP-116.

TYPICAL DEVICE CONTROL INTERFACE

Simplified logic of a typical I/O device control interface is shown in Figure11. The essential items are a group of address and function decoders, a ready flip-flop, a busy flip-flop, a mask flip-flop, an input/output mode flip-flop, and a data buffer. Additional logic may be added as required to accommodate special device controls or format conversion.

OCP Commands

An OCP from the DDP-116 consists of a device address and function code times with an OCP pulse. The interface address and function decoders respond to the OCP command by energizing appropriate device control lines, to set up the specified operating condition. In the case of a command of the "write" type (a data output from the DDP-116), both the ready and busy flip-flops are set. The interface is prepared to accept data immediately.

A command of the "read" type (a data input to the DDP-116) sets only the busy flip-flop; the ready flip-flop remains reset until the device drop-in pulse (DIP) has deposited data in the buffer register. An SKS instruction (or the SKS portion of an INA instruction) will then inform the DDP-116 that the input transfer can be performed.

The mode flip-flop is set up according to the type of OCP in effect, to store an indication of the direction of data transfer.

SKS Testing

During an SKS cycle, the address bus addresses the device, and the function code bits specify the condition to be tested. In the illustrated example, independent gates test for SKS ready, SKS busy, and SKS interrupt. Other SKS gates may be added as required to test for special device conditions, such as "end of file." When an SKS condition is fulfilled, the DRLXX-line is brought to 0 vdc.

Standard Input Data Transfers

An SKS ready test is provided as an integral part of the INA cycle. In a device with an inherent mechanical delay between a "start" command and the first character delivery, the waiting period may be utilized for computation. The ready flip-flop remains reset until the device drop-in pulse ($\overline{\text{DIP}}$) loads data into the buffer register. If, during an INA instruction, the DRLXX-line has not reached the "ready" condition, the DDP-116 ignores the input bus and continues with data processing. If during a subsequent test the DRLXX-line indicates that the input character is ready, the data is strobed in from the input bus. Gating of data to the input bus by the decoded device address guarantees that only one device will be connected to the input bus. When the ready condition permits an input transfer, the DDP-116 generates the RRLXX-pulse, during which the device buffer

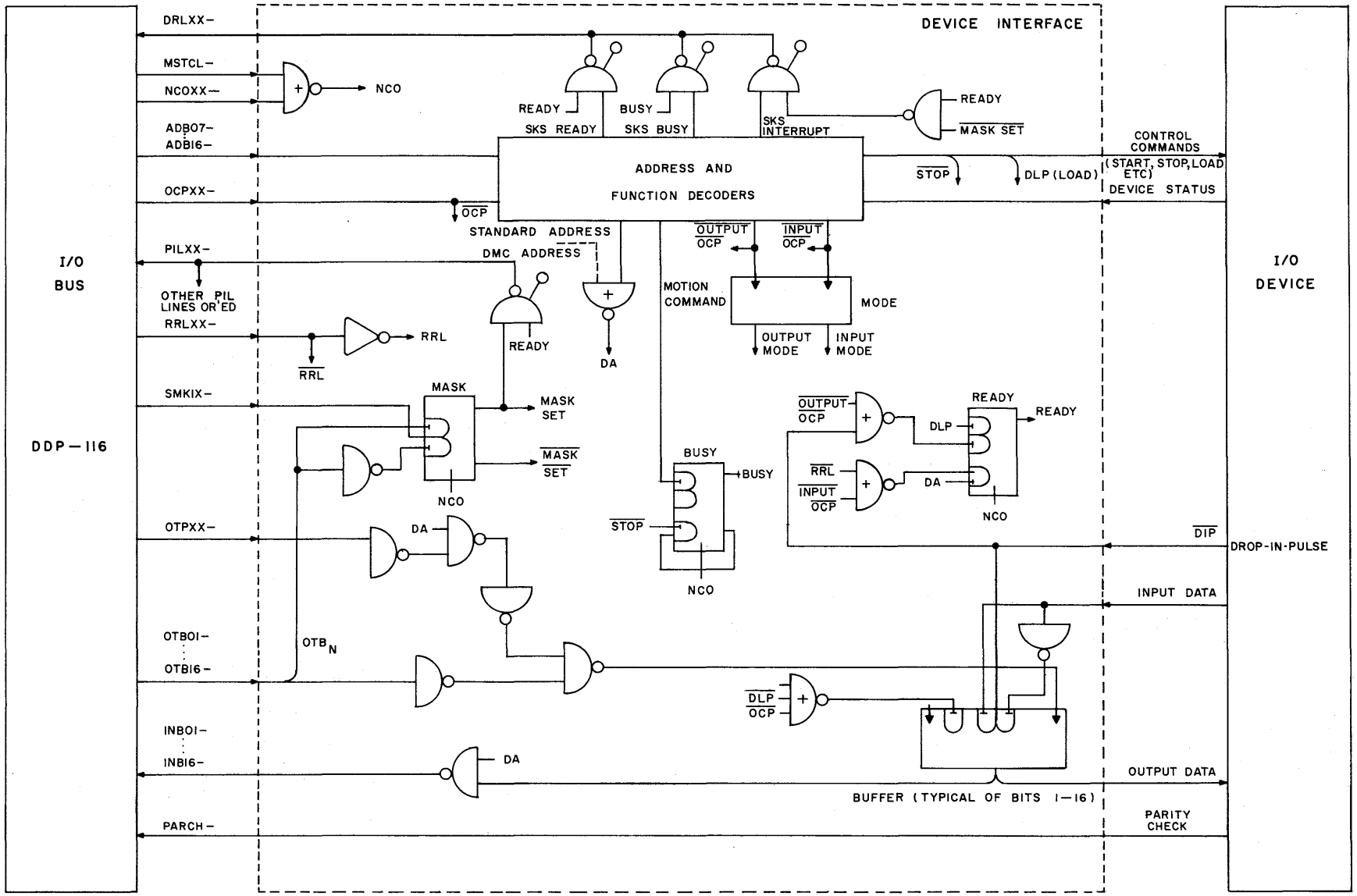

Figure 11. Typical Device Control Interface, Simplified Logic Diagram

and the ready flip-flop are reset in preparation for another cycle. Input transfers continue as long as the device is operating and INA instructions recur.

Standard Output Data Transfers

During the first of a series of OTA instructions, the ready flip-flop will be set, and the SKS test performed as part of the instruction will be satisfied. The first data word is strobed into the device buffer by the OTP pulse. The input/output mode flip-flop, set to the output mode condition by a previous OCP, prevents resetting of the buffer by the RRLXX-pulse. The resetting of the ready flip-flop by the trailing edge of the RRLXX-pulse renders the device exempt from I/O transfers until the character in the buffer has been taken during the device load pulse (DLP). The trailing edge of DLP again sets the ready flip-flop, after which another word can be loaded by the next OTA cycle.

Setting Mask Flip-Flop

Mask flip-flops for all devices on the standard I/O bus are set up simultaneously by a unique instruction that gates a mask code on the output bus and produces the SMK1X-pulse. Each device is assigned one output bus line; if that bit contains a binary ONE, the mask flip-flop is set; otherwise the mask flip-flop is reset. Note that the mask set instruction may be used to prevent interrupts as well as enable them.

Standard Interrupt for Input

After an OCP has enabled a device to provide input data to the DDP-116, the computer may continue with the normal program until the device drop-in pulse ($\overline{\text{DIP}}$) delivers the first word to the buffer and sets the ready flip-flop. The ready condition, gated with the set output of the mask flip-flop, energizes the PILXX-line. The energization of the PILXX-line forces the program to jump to a priority subroutine in which SKS interrupt instructions are addressed to the various peripheral devices in the order of priority. (Meanwhile, the interrupting device holds the data ready in the interface buffer.) An SKS interrupt command addressed to the active device is decoded and gated with $\overline{\text{MASK SET}}$ and READY. A negation on the DRLXX-line permits the DDP-116 to undergo a program jump to an INA instruction that will accept the data and reset the ready flip-flop. The next drop-in pulse again sets the ready flip-flop, and the cycle is repeated.

Standard Interrupt for Output

When an OCP has enabled a device to request data from the DDP-116, the device ready flip-flop is set concurrently, and, if the mask flip-flop is set, the PILXX-line is energized. The DDP-116 immediately enters a priority subroutine in which all peripheral devices are tested by an SKS interrupt in the order of priority. An SKS interrupt command

addressed to the active device is decoded and gated with $\overline{\text{MASK SET}}$ and READY. An assertion on the DRLXX-line permits the DDP-116 to undergo a program jump to an OTA instruction that will strobe data to the device buffer and reset the ready flip-flop. Removal of the ready condition deenergizes the PILXX-line. The device thus remains exempt from OTA data transfers until the device load pulse ($\overline{\text{DLP}}$) takes the data and sets the ready flip-flop. The PILXX-line is again energized and another interrupt cycle is requested.

System Normalize

Two lines from the computer place the device interface in a normal starting condition. The MSTCL-level is produced whenever the MASTER CLEAR button is pressed; the NCOXX-system normalize pulse occurs for 100 milliseconds at the beginning of every power-on cycle. Both signals are ORed in the interface and converted to the NCO level, which resets the busy, ready, and mask flip-flops.

Special DMC Provisions

Device interfaces may optionally be provided with subchannel logic for operation under DMC control. The required additions are a DMC enable flip-flop and control logic to produce the DILXX- DMC interrupt line. These elements are shown in Figure 12.

In DMC operation, the DMC address is used in lieu of the standard address to prepare the interface for a data transfer, either input or output. A DMC enable flip-flop, set by a special OCP command, enables DMC interrupt requests on the DILXX+line. When an ERLXX- end-of-range signal from the DMC option has reset the DMC ready flip-flop, DMC interrupts are not permitted.

Except for these provisions, DMC data transfers occur in the same manner and use the same I/O and control lines as the standard I/O bus.

Devices capable of block transfers must also have provisions for connection to the STOPX-line which resets the DMC block transfer control flip-flop when a device has run out of data before the end of range has been reached. Otherwise, the DMC would retain control and wait for nonexistent data.

Parity Check Input

A parity error signal input line, PARCH-, is provided on an I/O connector so that devices with parity check logic can light the parity error indicator on the DDP-116 control panel. To energize the indicator, a -6-volt input level is required.

SYSTEM INTERCONNECTING DATA

A typical expanded DDP-116 installation involving a main frame and satellite cabinet is shown in Figure 13. When rack-mounted devices are supplied as an integral part of an option cabinet, all interconnections are wire-wrapped upon initial assembly; no cabling is necessary.

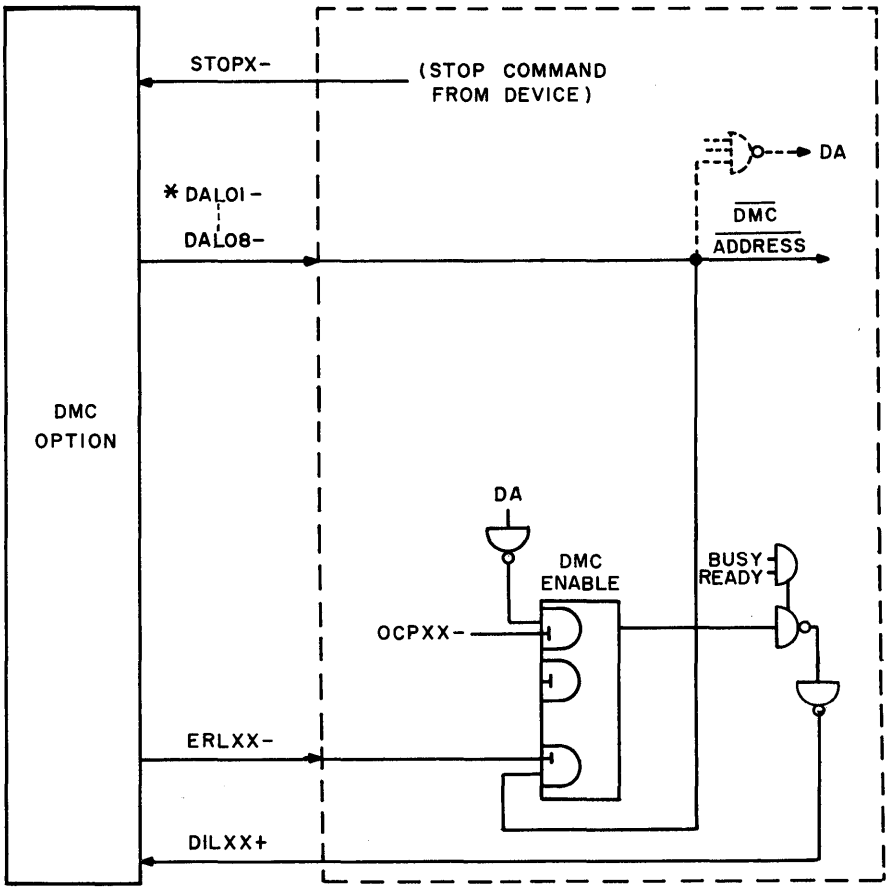

Figure 12. Additional Interface Logic Required for DMC Option

I/O bus communication from cabinet to cabinet is by means of umbilical I/O cables. Such cables are permanently wired to an option cabinet at one end; the other end is equipped with plugs that match standard I/O connector jacks. Any number of option cabinets may be interconnected in this manner.

Eight additional control lines, ACK01- through ACK08-, are provided to reset interrupt control flip-flops in devices that do not contain a ready flip-flop. (The Real Time Clock option is such a device.) Devices that are not involved in data transfers never receive INA or OTA commands and thus do not receive the RRLXX-pulse that resets the ready flip-flop and disables the PIL line.

The ACK lines are produced in the priority interrupt option by type S-169 Special PACs. Each line is capable of driving up to 16.8 ma at 0 volt but the recommended design

TELETYPE DATA LINE CONNECTION

SIGNAL	TELETYPE TERMINAL	POWER DISTRIBUTION BOX TERMINAL
ASR DATA	TB1-6	A2C1B-4
ASR-18V	TB1-7	A2C1B-6

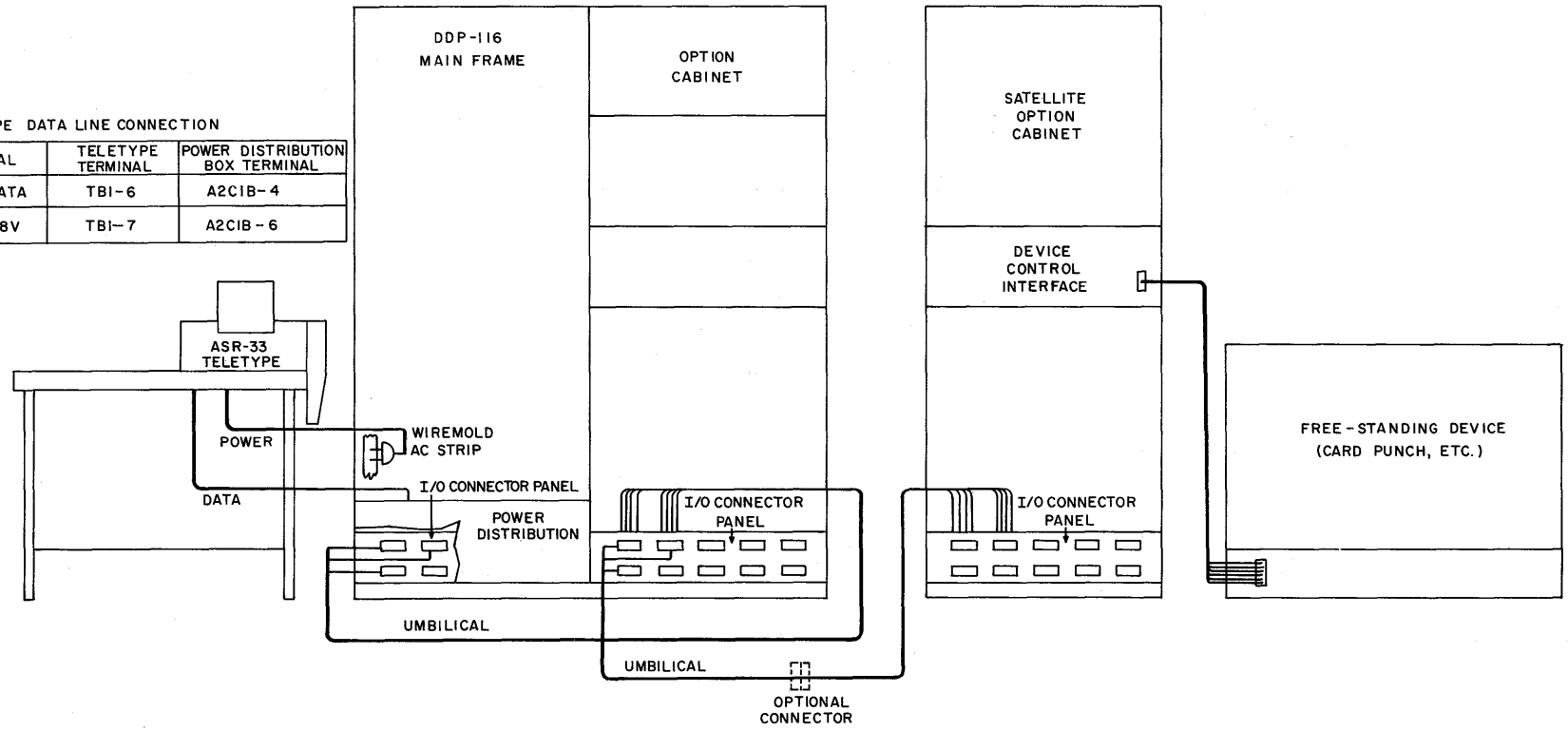

Figure 13. Rear View of Typical DDP-116 System Installation

load limit is 2.4 ma at 0 volt. The lines are brought to the negation level (0 volt) for approximately 2.0 μsec during the interrupt JST instruction cycle.

Interconnecting Cables

Interconnecting cables between the DDP-116 and peripheral equipment will vary in length according to the placement of the units with relation to each other. Maximum length of signal cables should be 50 ft. If cable lengths are specified in the contract, cables of the specified length will be provided with the equipment. If the cables are to be assembled at the installation site, mating plugs are provided for the receptacles of the connector panel.

A 15-ft power input cable is provided with each DDP-116 system. It is normally taped within the equipment for storage during shipment.

Power and data cables are supplied with the ASR-33 Teletype. The power cable plugs in to the main frame wiremold ac strip. The two-wire data cable attaches to a terminal block on the ASR-33.

I/O Connectors

The DDP-116 is equipped with a comprehensive connector panel, located behind the hinged ac power distribution chassis at the rear of the main enclosure. (See Figure 14.) All connectors on the panel are identical. Three (A2S1A, A2S2A, and A2S1B) are permanently allocated as I/O connectors, with the I/O bus pin assignments listed in Tables 8, 9, and 10. Another connector, A2S2B,(Table 11), is provided for control lines used with the priority interrupt option. Remaining connector cutouts on the panel are for connectors required by special systems. Information on special connector pin assignments will be supplied as required.

Extension and satellite enclosures are identically equipped with a standard connector panel.

AC Power Distribution

AC line power is distributed within the standard DDP-116 through a wiremold receptacle strip running the vertical length of the cabinet. Power supplies, blowers, and other devices requiring line power are converted directly into the strip. Prime power is controlled by circuit breakers and contactors in the power distribution box.

DC Power Distribution

DC power from the RP-60 power supply in the standard DDP-116 is distributed within the enclosure by laminated copper strip conductors running vertically to the right of the S-BLOCs. Smaller copper bus strips carry voltages horizontally to standard pins of the S-PAC connectors. No cabling is required.

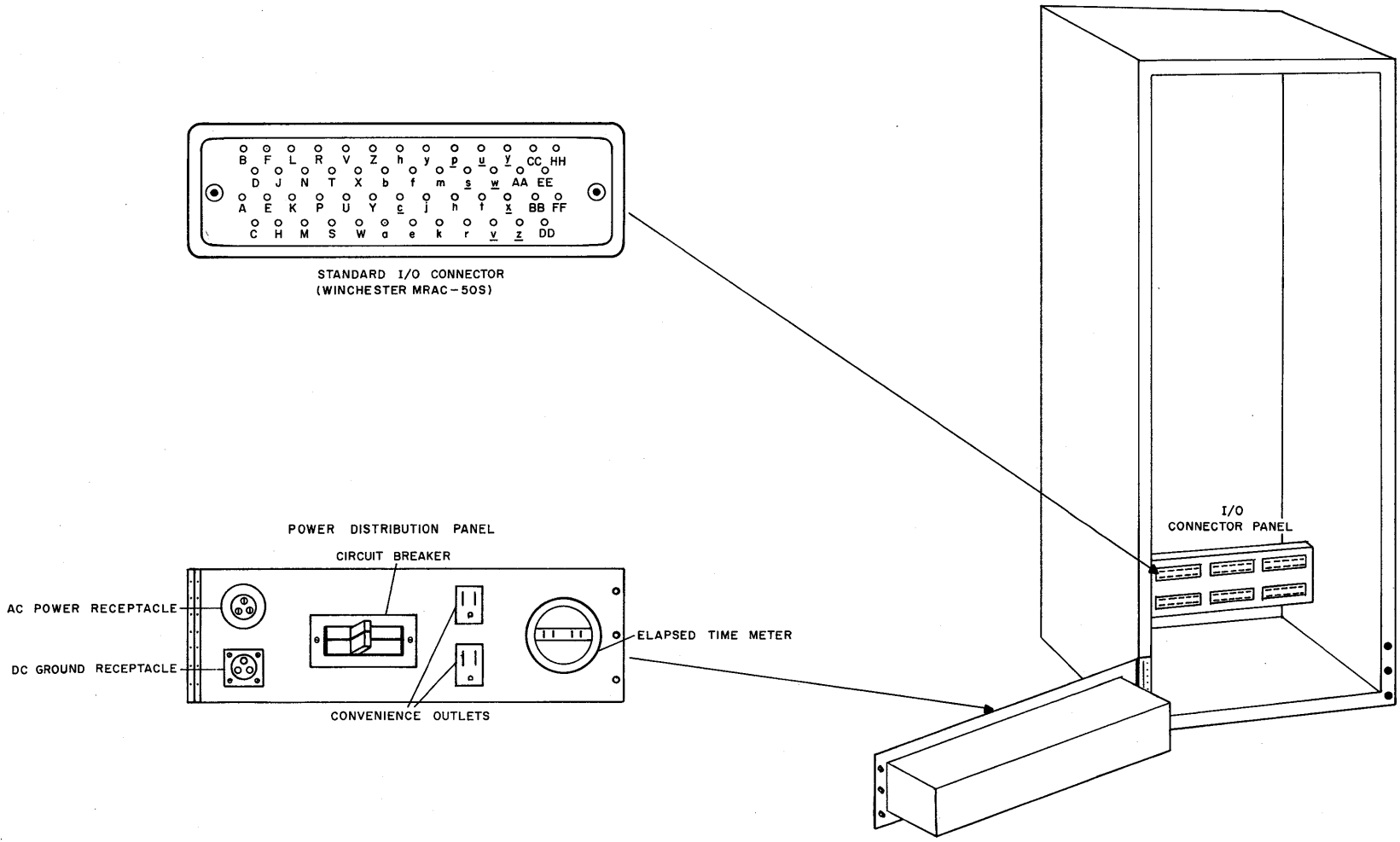

Figure 14. DDP-116 I/O Connectors

System Grounding

AC power ground is brought into the DDP-116 enclosure in the main power cable. DC power ground is distributed within the enclosure by a copper comb running along the bottom of each S-BLOC. A common dc ground is maintained from cabinet to cabinet by using the dc ground connector, A2B2D.

Table 8.
Standard I/O Connector A2S1A Pin Assignments

Pin	Function	Pin	Function
A	OTB01-	e	OTB14-
B	OTB01-GND	f	OTB14-GND
C	OTB02-	h	OTB15-
D	OTB02-GND	j	OTB15-GND
E	OTB03-	k	OTB16-
F	OTB03-GND	m	OTB16-GND
H	OTB04-	n	DRLXX-
J	OTB04-GND	p	DRLXX-GND
K	OTB05-	r	
L	OTB05-GND	s	
M	OTB06-	t	
N	OTB06-GND	u	
P	OTB07-	v	
R	OTB07-GND	w	
S	OTB08-	x	
T	OTB08-GND	y	
U	OTB09-	z	
V	OTB09-GND	AA	
W	OTB10-	BB	
X	OTB10-GND	CC	
Y	OTB11-	DD	
Z	OTB11-GND	EE	
a	OTB12-	FF	
b	OTB12-GND	HH	
c	OTB13-		
d	OTB13-GND		

Table 9.
Standard I/O Connector A2S2A Pin Assignments

Pin	Function	Pin	Function
A	INB01-	e	INB14-
B	INB01-GND	f	INB14-GND
C	INB02-	h	INB15-
D	INB02-GND	j	INB15-GND
E	INB03-	k	INB16-
F	INB03-GND	m	INB16-GND
H	INB04-	n	
J	INB04-GND	p	
K	INB05-	r	OTPXX-
L	INB05-GND	s	OTPXX-GND
M	INB06-	t	RRLXX-
N	INB06-GND	u	RRLXX-GND
P	INB07-	v	OCPXX-
R	INB07-GND	w	OCPXX-GND
S	INB08-	x	PILXX+
T	INB08-GND	y	PILXX+GND
U	INB09-	z	SMK1X-
V	INB09-GND	AA	SMK1X-GND
W	INB10-	BB	SMK2X-
X	INB10-GND	CC	SMK2X-GND
Y	INB11-	DD	SMK3X-
Z	INB11-GND	EE	SMK3X-GND
a	INB12-	FF	SMK4X-
b	INB12-GND	HH	SMK4X-GND
c	INB13-		
d	INB13-GND		

Table 10.
Standard I/O Connector A2S1B Pin Assignments

Pin	Function	Pin	Function
A	ADB07-	e	DIL04+
B	ADB07-GND	f	DIL04+GND
C	ADB08-	h	DIL05+
D	ADB08-GND	j	DIL05+GND
E	ADB09-	k	DIL06+
F	ADB09-GND	m	DIL06+GND
H	ADB10-	n	DIL07+
J	ADB10-GND	p	DIL07+GND
K	ADB11-	r	DIL08+
L	ADB11-GND	s	DIL08+GND
M	ADB12-	t	
N	ADB12-GND	u	
P	ADB13-	v	
R	ADB13-GND	w	
S	ADB14-	x	PARCH-
T	ADB14-GND	y	PARCH-GND
U	ADB15-	z	ERLXX-
V	ADB15-GND	AA	ERLXX-GND
W	ADB16-	BB	MSTCL-
X	ADB16-GND	CC	MSTCL-GND
Y	DIL01+	DD	NCOXX-
Z	DIL01+GND	EE	NCOXX-GND
a	DIL02+	FF	STOPX-
b	DIL02+GND	HH	STOPX-GND
c	DIL03+		
d	DIL03+GND		

Table 11.
Standard I/O Connector A2S2B Pin Assignments

Pin	Function	Pin	Function
A	DAL01-	e	ACK05-
B	DAL01-GND	f	ACK05-GND
C	DAL02-	h	ACK06-
D	DAL02-GND	j	ACK06-GND
E	DAL03-	k	ACK07-
F	DAL03-GND	m	ACK07-GND
H	DAL04-	n	ACK08-
J	DAL04-GND	p	ACK08-GND
K	DAL05-	r	PIL01+
L	DAL05-GND	s	PIL01+GND
M	DAL06-	t	PIL02+
N	DAL06-GND	u	PIL02+GND
P	DAL07-	v	PIL03+
R	DAL07-GND	w	PIL03+GND
S	DAL08-	x	PIL04+
T	DAL08-GND	y	PIL04+GND
U		z	PIL05+
V		AA	PIL05+GND
W	ACK01-	BB	PIL06+
X	ACK01-GND	CC	PIL06+GND
Y	ACK02-	DD	PIL07+
Z	ACK02-GND	EE	PIL07+GND
a	ACK03-	FF	PIL08+
b	ACK03-GND	HH	PIL08+GND
c	ACK04-		
d	ACK04-GND		